## REMARKS

Applicant appreciates the thorough examination of the application that is reflected in the Office Action dated January 23, 2003. Claims 1 and 18 are amended to correct informalities and to use proper English phraseology; marked up versions of the amended claims are attached hereto pursuant to 37 C.F.R. § 1.121(c)(ii). These amendments do not alter the scope of claims 1 and 18. Claims 1-18 are pending in the application. Reexamination and reconsideration of the application, as amended, are respectfully requested.

**Drawings**

Submitted herewith is a proposed drawing correction with proposed changes marked in red ink. Specifically, a –Prior Art – legend has been added to each of FIGS. 10A-11C. Accordingly, the objection to the drawings is moot.

**Claim Rejections Under 35 U.S.C. 112, 1st Paragraph**

Claims 7-8 and 16 were rejected under 35 U.S.C. 112, first paragraph.

Applicant notes that dependent claims 6 and 7 both depend from claim 1, while claims 15 and 16 both depend from claim 10. Applicant traverses this rejection and submits that claims 7 and 16 are supported throughout the specification and drawings, for instance, by the text at page 21, lines 11-21 and page 29, lines 16-21, as well as by claims 7 and 16 which were filed with the original application. Accordingly, Applicant submits that the rejection of claims 7-8 and 16 under 35 U.S.C. 112, first paragraph was improper and requests that this ground of rejection be withdrawn.

**Claims 1, 9, 10, and 18**

Claims 1, 2, 6, 9-11, 15 and 18 were rejected under 35 U.S.C. 102(b) as being anticipated by Iwasaki et al. (hereinafter "Iwasaki") and claims 1, 2, 6-11, and 15-18 were rejected under 35 U.S.C. 102(b) as being anticipated by EP Patent Application Number 0,558,059 to Ishizaki et al (hereinafter "Ishizaki").

Claim 18 relates to a driving method, comprising:

> supplying a scanning signal including a scanning period in which at least one of a plurality of scanning lines is selected, to the plurality of scanning lines by scanning line driving circuit; and
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> supplying a data signal to a plurality of pixel electrodes by data line driving circuit through N columns of data lines and a plurality of switching elements connected to the at least one selected scanning line; and

by polarity inversion driving circuit, inverting a polarity of a voltage applied to the liquid crystal layer, which is formed between the pixel electrodes and the opposite electrode, by changing a voltage supplied to an opposite electrode of a row corresponding to the selected scanning line in synchronization with the scanning period. (Emphasis added.)

Applicant submits that the cited references fail to teach or suggest all of the recitations of claim 18. The cited references all fail to teach or suggest, for example, that "changing a voltage supplied to an opposite electrode of a row corresponding to the selected scanning line in synchronization with the scanning period," as required by claim 18.[1]

For example, the cited portion of Iwasaki at col. 13, line 26- col. 14, line 51, discusses waveform diagrams of drive voltages when odd row and even row pixels are driven. Iwasaki is silent with respect to polarity inversion "by changing a voltage supplied to an opposite electrode of a row corresponding to the selected scanning line in synchronization with the scanning period." Ishizaki discloses the concept of a third shift register 103 for driving opposite electrodes, but fails to disclose "changing a voltage supplied to an opposite electrode ... **in synchronization with the scanning period**," as required by claim 18.

Applicant therefore respectfully submits that claim 18 is patentable over the cited references for at least the foregoing reasons. Applicant also submits that independent claims 1, 8, 9, and 10 are also patentable for at least the same reasons. Applicant further submits that claims 2-7 and 11-16 are patentable at least by virtue of their dependency from claims 1 and 10,respectively.

**Claims 2 and 11**

Claim 2 depends from claim 1, and is therefore patentable at least by virtue of its dependency from claim 1. In addition, Applicant respectfully submits that the cited references fail to teach or suggest that the polarity inverting circuit "inverts a voltage supplied to the opposite electrodes for the respective rows in synchronization with a beginning of the scanning

[1] Exemplary benefits associated with changing a voltage supplied to an opposite electrode of a row corresponding to the selected scanning line in synchronization with the scanning period are discussed, for example, at page 11, lines 15-20, page 21, lines 11-21, and page 23, line 18 through page 24, line 8 of the present application. Applicant notes, however, that the claims are not to be construed as being limited by these embodiments.

period," as required by claim 2. [2] Accordingly, the rejection of claim 2 based on the cited references should also be withdrawn. Applicant further submits that claim 11 is also separately patentable for at least the same reasons. In the event, the Examiner seeks to maintain the rejection of claims 2 and 11, Applicant respectfully requests that the Examiner describe how the cited references teach or suggest this limitation.

**Claims 6 and 15**

Claim 6 depends from claim 1, and is therefore patentable at least by virtue of its dependency from claim 1. In addition, Applicant respectfully submits that the cited references fail to teach or suggest that the polarity inverting circuit "the polarity inverting circuit inverts a polarity of a voltage applied to the liquid crystal layer every one frame," as required by claim 6. Accordingly, the rejection of claim 6 based on the cited references should also be withdrawn. Applicant further submits that claim 15 is also separately patentable for at least the same reasons. In the event, the Examiner seeks to maintain the rejection of claims 6 and 15, Applicant respectfully requests that the Examiner describe how the cited references teach or suggest this limitation.

**Claims 7 and 16**

Claim 7 depends from claim 1, and is therefore patentable at least by virtue of its dependency from claim 1. In addition, Applicant respectfully submits that the cited references fail to teach or suggest that the polarity inverting circuit "the polarity inverting circuit inverts a polarity of a voltage applied to the liquid crystal layer for each one of the M rows of scanning lines," as required by claim 7. Accordingly, the rejection of claim 7 based on the cited references should also be withdrawn. Applicant further submits that claim 16 is also separately patentable for at least the same reasons. In the event, the Examiner seeks to maintain the rejection of claims 7 and 16, Applicant respectfully requests that the Examiner describe how the cited references teach or suggest this limitation.

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[2] Exemplary benefits associated with this aspect are discussed, for example, at page 11, line 24 – page 12, line 2, and page 28, line 21 through page 29, line 2 of the present application. Applicant notes, however, that the claims are not to be construed as being limited by these embodiments.

**Claims 8 and 17**

Claims 8 and 17 were rejected under 35 U.S.C. 102(b) as being anticipated by EP Patent Application Number 0,558,059 to Ishizaki et al (hereinafter "Ishizaki").

Applicant submits that the cited references fail to teach or suggest, for example, that "the substrate includes M rows of opposite electrodes, each of said row of said opposite electrodes arranged oppositely a row of the M X N number of pixel electrodes in a rectangular shape, wherein the M rows of opposite electrodes are insulated from each other," as required by claim 17.[3] Applicant therefore respectfully submits that claim 17 is patentable over the cited references for at least the foregoing reasons.

Claim 8 depends from claims 1-7, and is therefore patentable at least by virtue of its dependency from claim 1. In addition, Applicant submits that claim 8 is also separately patentable for at least the same reasons discussed above with respect to claim 17.

Accordingly, the rejection of claims 8 and 17 based on the cited references should also be withdrawn. In the event, the Examiner seeks to maintain the rejection of claims 8 and 17, Applicant respectfully requests that the Examiner describe how the cited references teach or suggest this limitation.

**Claims 3, 4, 5 and 12, 13, 14**

Claims 3-5 and 12-14 were rejected under 35 U.S.C. 103(a) as being unpatentable over Ishizaki in view of U.S.P.N. 4,394,380 to Hosokawa et al.

Claims 3-5 depend directly or indirectly from claim 1, and are therefore patentable at least by virtue of their dependency from claim 1. In addition, Applicant respectfully submits that the cited references fail to teach or suggest "a memory section which holds a first electric potential or a second electric potential as an electric potential for each of the M rows of opposite electrodes, and updates the held electric potential every scanning period; and an electric potential selecting circuit for selecting the electric potential supplied to the M rows of opposite electrodes

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[3] Exemplary benefits associated with this aspect are discussed, for example, at page 13, lines 5-17 and page 29, lines 9-15 of the present application. Applicant notes, however, that the claims are not to be construed as being limited by these embodiments.

based on the first electric potential or the second electric potential outputted from the memory section every scanning period," as required by claim 3. [4]

The Examiner concedes that Ishizaki et al. fail to disclose all of the limitations required by claims 3 and 12. The Examiner cites Hosokawa et al. as teaching this feature. However, FIG. 4, col.7, line 35 through col. 8, lines 8 simply teach a common driver having a shift register, and does not teach "a memory section which holds a first electric potential or a second electric potential as an electric potential for each of the M rows of opposite electrodes, and updates the held electric potential every scanning period; and an electric potential selecting circuit for selecting the electric potential supplied to the M rows of opposite electrodes based on the first electric potential or the second electric potential outputted from the memory section every scanning period," as required by claims 3 and 12.

Applicant also respectfully submits that the cited references fail to teach or suggest that "the memory section is a shift register which sequentially shifts an input signal of the first electric potential or the second electric potential," as required by claim 4. [5] In addition, Applicant respectfully submits that the cited references fail to teach or suggest that "the scanning line driving circuit sequentially switches a scanning line selected in synchronization with a clock signal, and wherein the shift register sequentially shifts the input signal in synchronization with the clock signal," as required by claim 5.

Accordingly, Applicant submits that claims 3-5 are separately patentable, and requests that the rejection of claims 3-5 based on the cited references be withdrawn. Applicant further submits that claims 12-14 are also separately patentable for at least the same reasons.

The art made of record but not relied upon by the Examiner has been considered. However, it is submitted that this art neither describes nor suggests the presently claimed invention.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

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[4] Exemplary benefits associated with this aspect are discussed, for example, at page 12, lines 13-15, and page 18, lines 2-9 of the present application. Applicant notes, however, that the claims are not to be construed as being limited by these embodiments.

[5] Exemplary benefits associated with this aspect are discussed, for example, at page 12, lines 19-24 of the present application. Applicant notes, however, that the claims are not to be construed as being limited by these embodiments.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6793 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,

HOGAN & HARTSON L.L.P.

Date: April 23, 2003

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**Version with markings to show changes made:**

1. (Amended) A liquid crystal device, comprising:

M rows of scanning lines, wherein [() M is an integer equal to or greater than 2[) rows of scanning lines], and N columns of data lines, wherein [()N is an integer equal to or greater than 2[) columns of data lines];

M X N number of switching element respectively connected to one of the M rows of scanning lines and one of the N columns of data lines;

M X N number of pixel electrodes respectively connected to one of the M X N number of switching element;

M rows of opposite electrodes arranged oppositely to respective rows of the M X N number of pixel electrodes through a liquid crystal layer;

a scanning line driving circuit [which supplies] configured to supply a scanning signal including a scanning period for selecting at least one of the M rows of scanning lines to the M rows of scanning lines;

a data line driving circuit [which supplies] configured to supply a data signal to the N columns of data lines; and

a polarity inverting circuit [which supplies] configured to invert a polarity of a voltage applied to the liquid crystal layer by changing a voltage supplied to an opposite electrode of a row corresponding to the selected scanning line in synchronization with the scanning period.

18. (Amended) A driving method, comprising:

[a step of] supplying a scanning signal including a scanning period in which at least one of a plurality of scanning lines is selected, to the plurality of scanning lines by scanning line driving circuit; and

[a step of] supplying a data signal to a plurality of pixel electrodes by data line driving circuit through N columns of data lines and a plurality of switching elements connected to the at least one selected scanning line; and

by polarity inversion driving circuit, [a step of] inverting a polarity of a voltage applied to the liquid crystal layer, which is formed between the pixel electrodes and the opposite electrode, by changing a voltage supplied to an opposite electrode of a row corresponding to the selected scanning line in synchronization with the scanning period.